IDEC Chip Design Contest

A Two-Phase Flying Capacitor Buck Converter with Enhanced Current Balancing Using Adaptive Dead-Time Control

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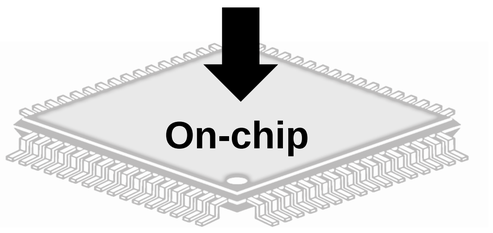
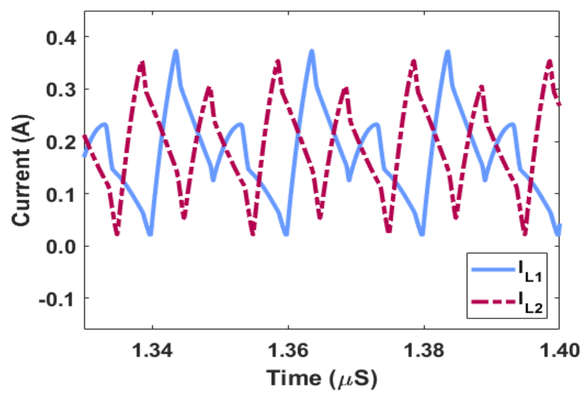
Introduction

(a)

Buck converter
+
Passive components



(b)

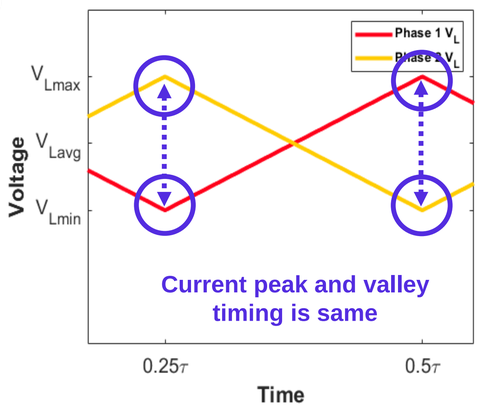


▲ (a) Concept of FIVRs and (b) Multi-phase flying capacitor buck converter current imbalance waveform.

- **Why fully integrated buck converter?**
  - Fast transient response for DVFS.
- **Key Features of Multi-Phase Technology in FIVRs**
  - Efficient current distribution: Each phase operates in parallel phases to handle high currents.
  - Reduced current ripple: Activate phases at $\frac{360°}{n}$ intervals to minimize output ripple.
  - Fast transient response: Provide rapid load regulation during dynamic changes.
- **Challenges in Multi-Phase Technology & Flying capacitor**
  - Current imbalance causes reduced efficiency, increased ripple, and elevated heat dissipation.
- **Proposed Idea**
  - Adaptive dead-time controller: To address timing mismatch and reduce current imbalnce.

Key Concepts in Current balancing

(a)



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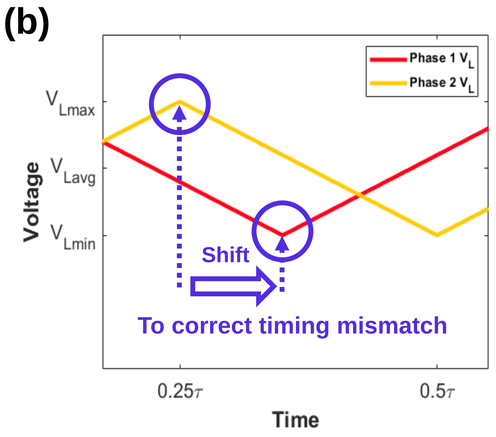
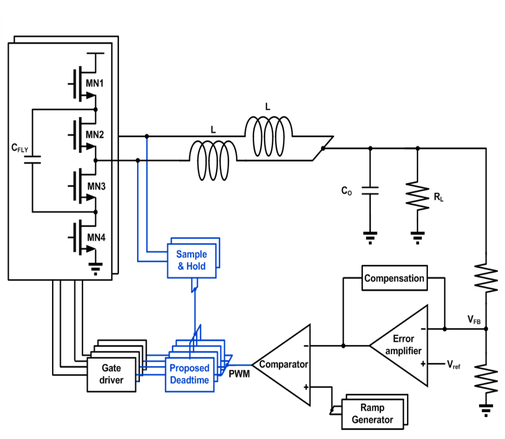


▲ Two-phase buck converter inductor current: (a) Ideal, (b) Non-idea.

- Controlling the dead-time of each phase corrects the timing mismatch between the inductor current peak and valley, effectively reducing current imbalance.

Operating Principles

(a)



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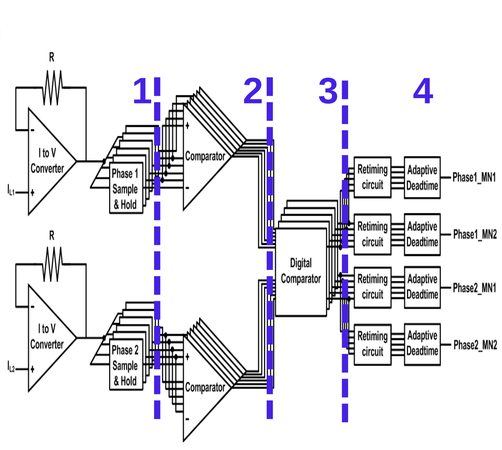
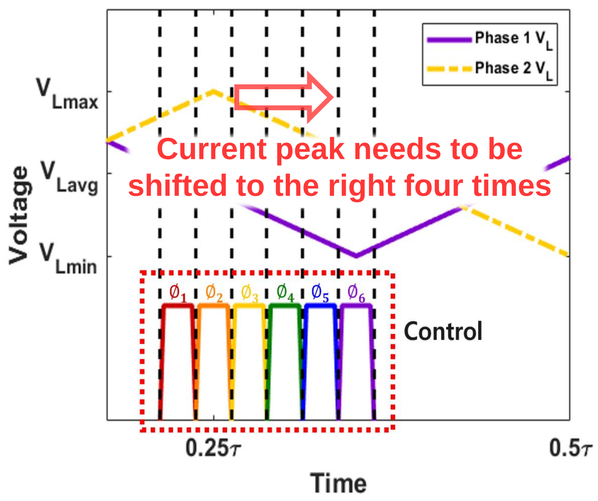


▲ Block diagram of (a) two-phase flying capacitor buck converter, (b) Adaptive dead-time controller.

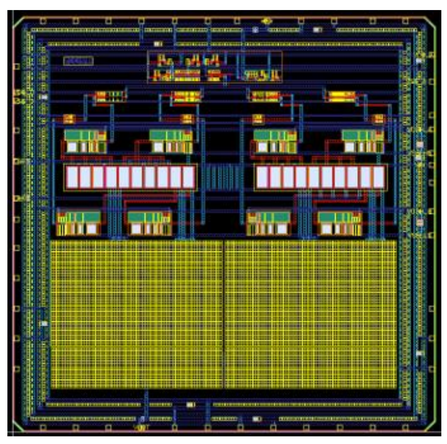


▲ Operation waveform

1. **Sample & Hold**
   - Sample each phase of the inductor current for six times
2. **Peak and valley detector**
   - Detect the inductor current peak and valley
3. **Timing mismatch detector**
   - Detect the timing mismatch of peak and valley
4. **Adaptive dead-time controller**
   - Control the dead-time

Layout & Results

(a)



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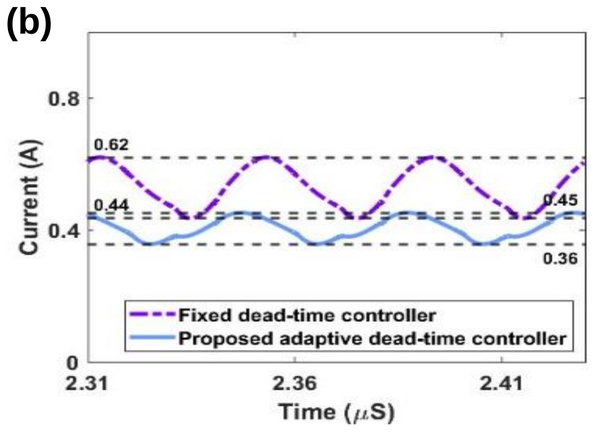

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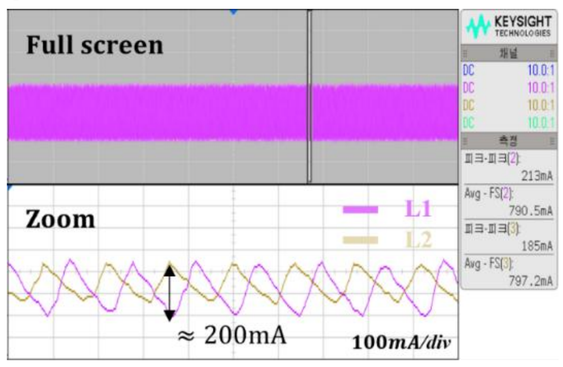
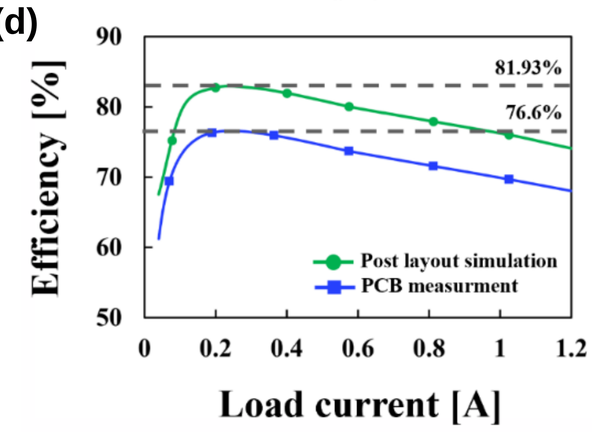


(d)



▲ (a) Circuit layout, (b) Current ripple: conventional vs. proposed (post-layout), (c) Two-phase inductor currents, (d) Efficiency: simulation vs. measurement.

- **Performance**
  - Phase current ripple: 90 mA (Post-layout), 200mA (PCB).
  - L1 and L2 operate with a 180° phase shift, achieving uniform current sharing.

Dead-time controller	Fixed	Adaptive
$I_{OUT,MAX}$ (mA)	620	450
$I_{OUT,MIN}$ (mA)	440	360
$I_{OUT,AVG}$ (mA)	530	400
ΔI_{OUT}	180	90 (-50%)

▲ Current ripple comparison.

Parameter	Post layout	PCB
V_{IN}(V)	5	5.5
V_{OUT}(V)	0.95	0.95
f_{sw}(MHz)	25	25
L(nH)	35	35
C_{FLY}(nF)	5	5
C_{OUT}(nF)	3	3
$I_{O,max}$(A)	2.3	1.2
η_{peak}(%)	81.93	76.6

▲ Performance comparison.

- **Discussion**
  - PCB measurement shows increased ripple (~200 mA) due to parasitic elements.
  - Input voltage raised to 5.5 V in measurement to compensate IR drop.
  - Efficiency drop (76.6%) attributed to parasitics and on-chip capacitor limitations.

Conclusion

- A two-phase IVR was implemented in 180 nm with an effective switching frequency of 50 MHz using a flying capacitor structure.
- Measured results showed stable 1.2 A operation and 76.6% peak efficiency with well-balanced phase currents.